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13		U.	S. PATENT I	DOCUMENTS			_l	
Exampleun							Filing D	16
Initials	1	Document Number	Date	Name	Class	Subclass	Filing Da	
DA	AA	5,821,014	10/13/1998	Chen et al	-		+	
)	AB	5,869,880	02/09/1999	Grill et al	 \ 		 	
	AC	5,936,295	08/10/1999	Havemann et al	 \		 	
	AD	6,083,275	07/04/2000	Heng et al		/		
	AE	6,252,290	06/26/2001	Quek et al	 	X	 	
	AF	6,277,728	08/21/2001	Ahn et al	 	\	 	
DI	AG	6,297,125	10/02/2001	Nag et al	 / 		<u> </u>	
	AH	3,27,420	10/02/2001	Trug or al			ļ	
	AI						 	
	1				<u></u>		<u> </u>	
FOREIGN PATENT DOCUMENTS								
	-	Document Number	Date	Country	Class	Subclass	Transla	tion
		2002					Yes	No
Þz.	AJ	1 152 463	11/07/2001	Europe				
ST /	AK	199 57 302	05/31/2001	Germany			See AP	
80	AL	101 09 778	09/19/2002	Germany				X
	AM				1	-	 	
	AN							
	AO				l			-
OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
AP United States Patent Application Publication no. US 2001/0002732 of Schwarzl et al,								
		published June 7, 2001						
i i	AQ	M.T. Bohr, "Interconnect Scaling - The Real Limiter to High Performance ULSI", IEDM						
-	AR	95, pages 241 – 244 S. Oh and K. Chang. "2001 Needs for Multi-Level Interconnect Technology". Giraita 8						
\		S. Oh and K. Chang, "2001 Needs for Multi-Level Interconnect Technology", Circuits & Devices, January 1995, pages 16 - 20						
	AS	T.H. Ning, "0.1 µm Technology and BEOL", Mat. Res. Soc. Symp. Proc., Vol. 427, 1996,						
		pages 17 – 21						
	ΑT	K. Yamashita & S. Odanaka, "Interconnect Scaling Scenario using a Chip Level Interconnect Model", Symp. On VLSI Technology Digest of Technical Papers, 1997, pages 53 - 54.						
\								
\	AU	Ueda et al, "A Novel Air Gap Integration Scheme for Multi-Level Interconnects Using Self-Aligned Via Plugs", 1998 Symposium on VLSI Technology Digest of Technical						
Pr/								
Papers, pp 46, 47.								
Examiner Date Considered								
7/10/04								
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609.								
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